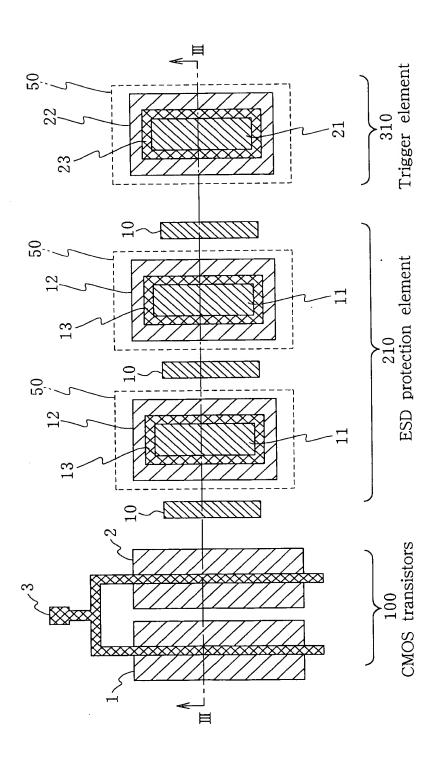


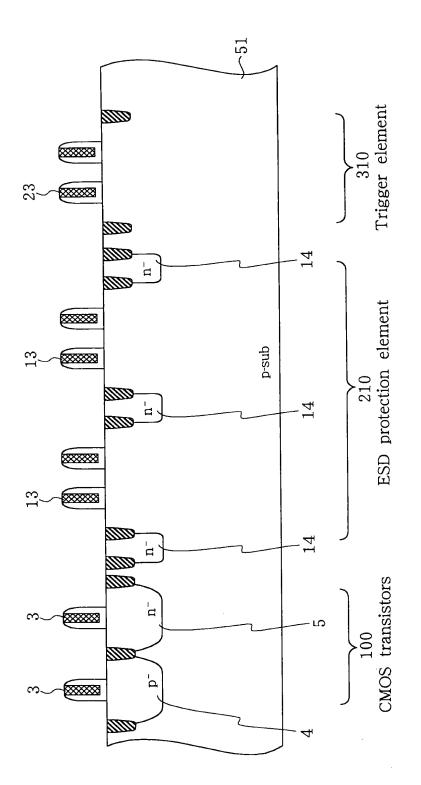
THE REPORT OF THE PARTY OF THE

FIG.1



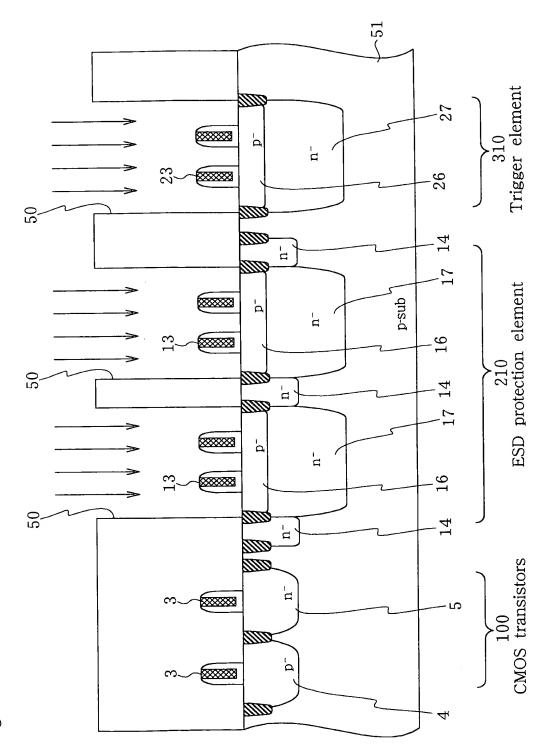
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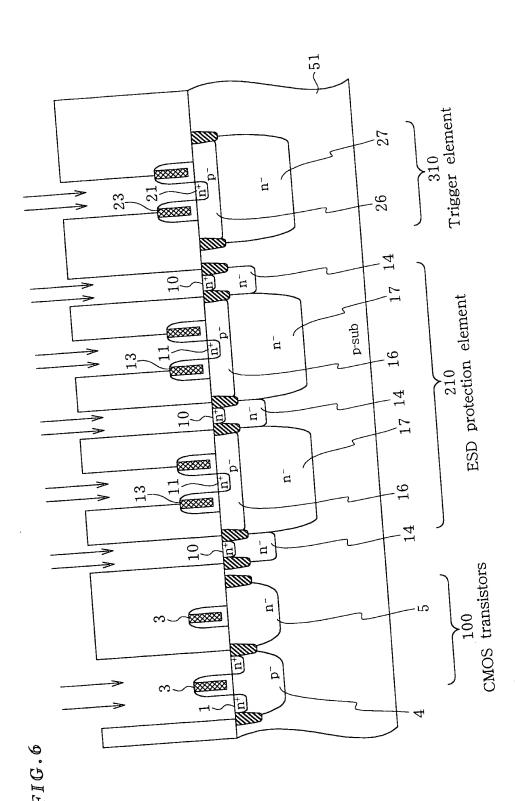
FIG. A

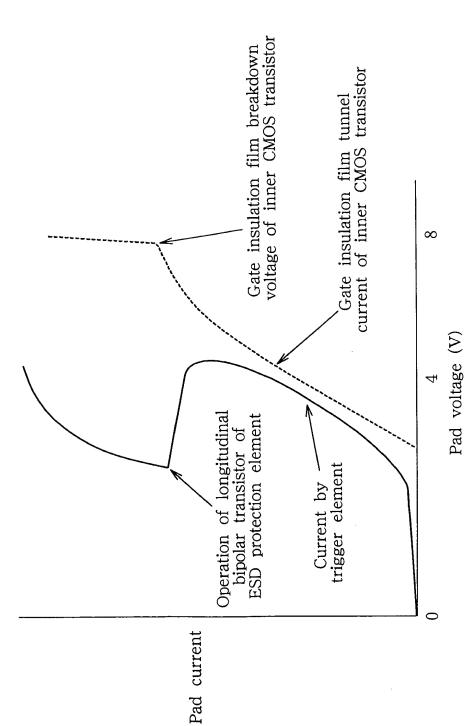


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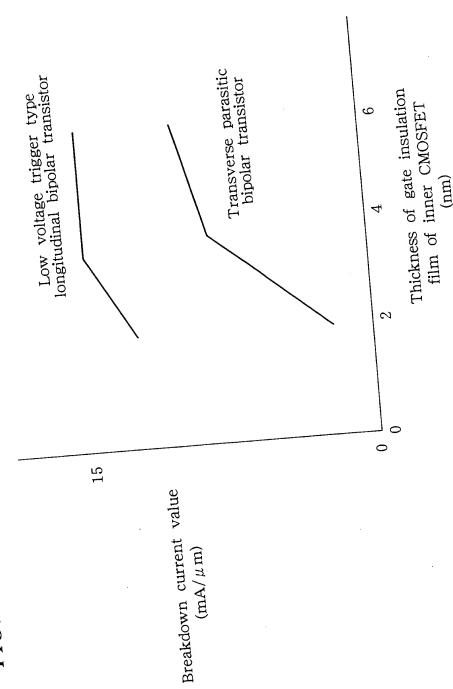


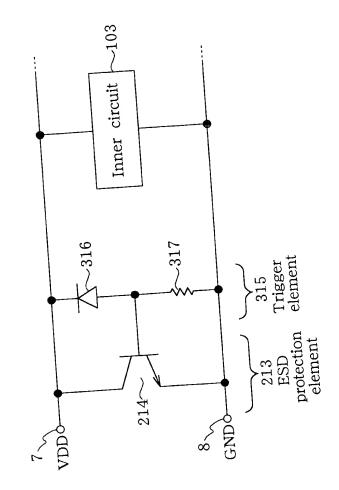




gate insulation film breakdown voltage of inner CMOS transistor Operation voltage of longitudinal bipolar transistor







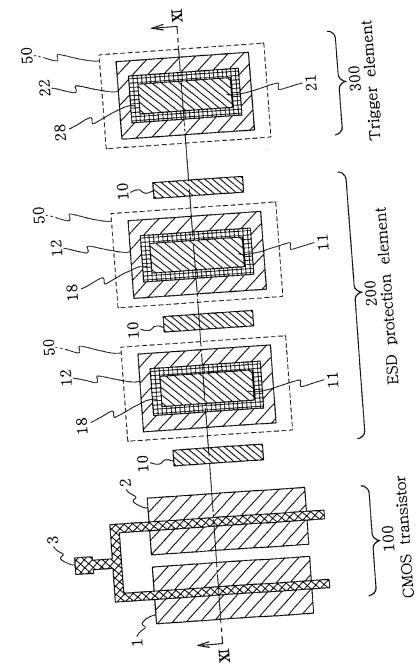


FIG.10

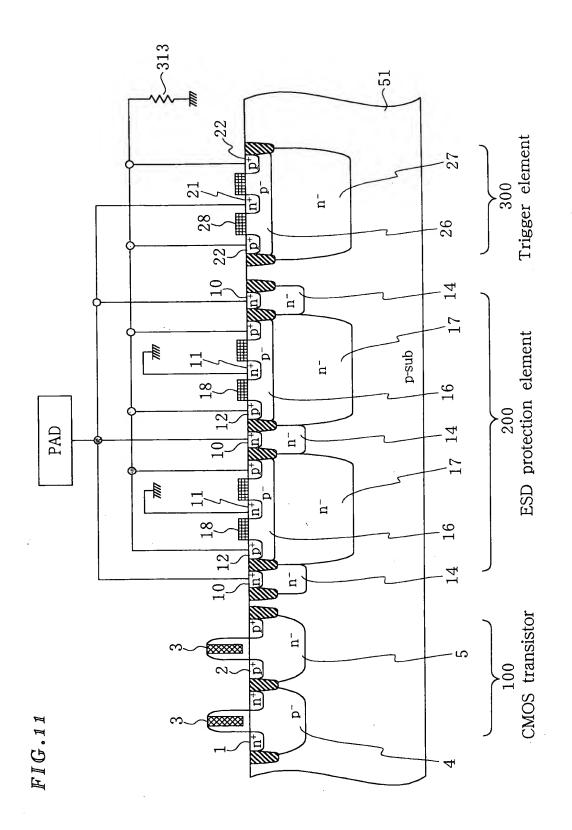
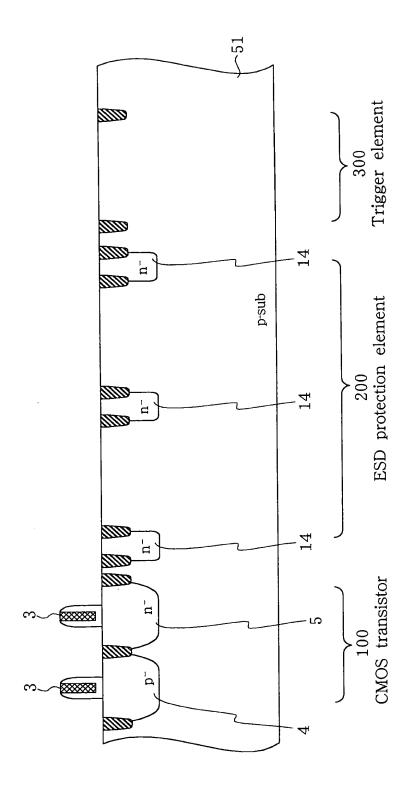
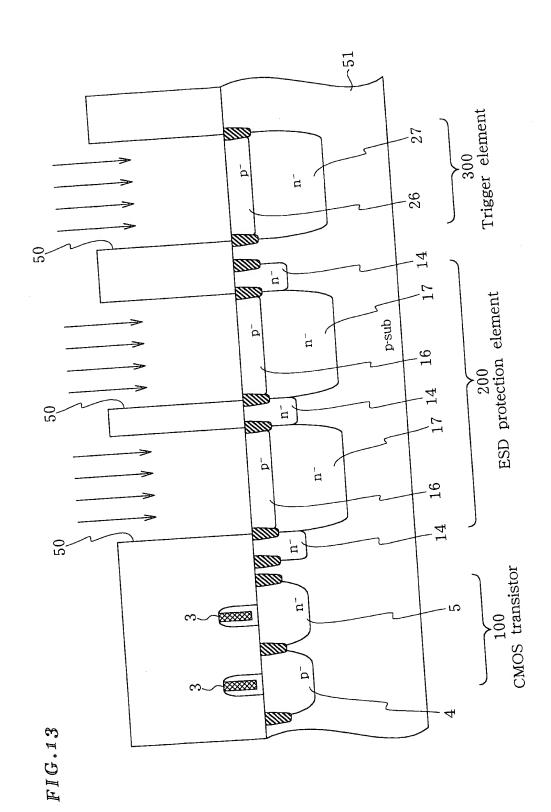
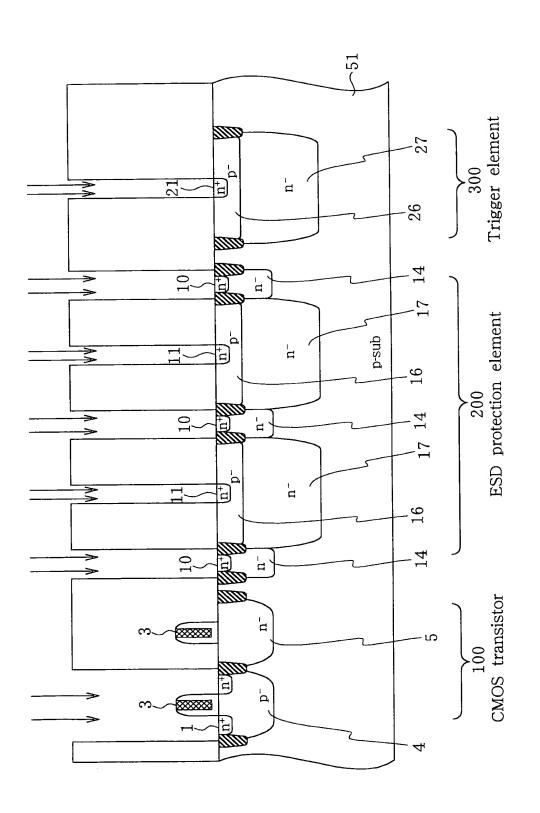


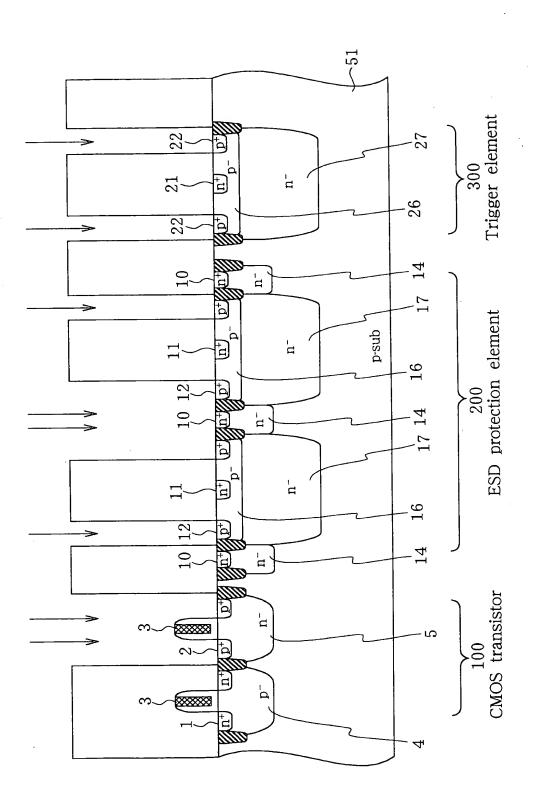
FIG.12











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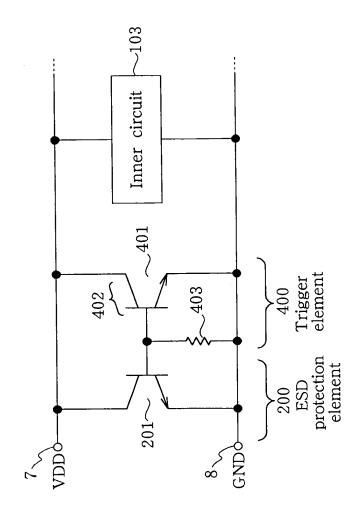
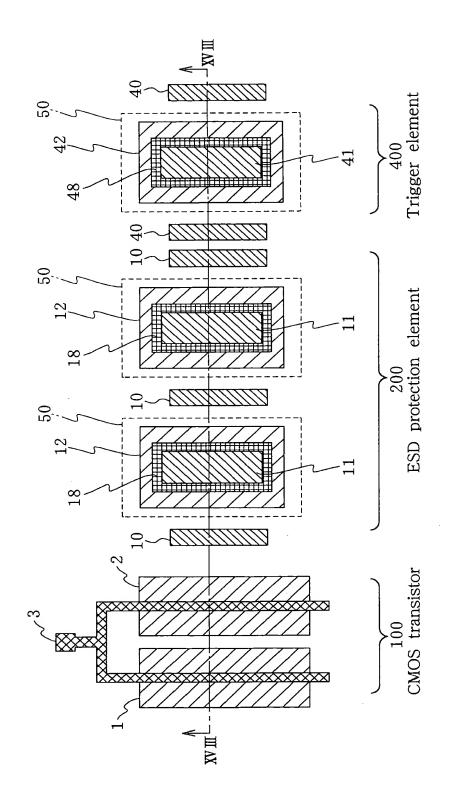
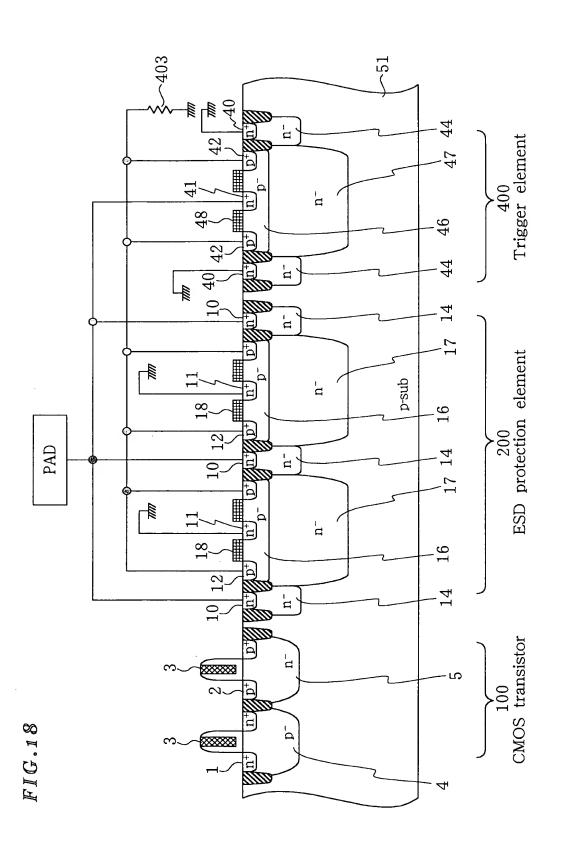
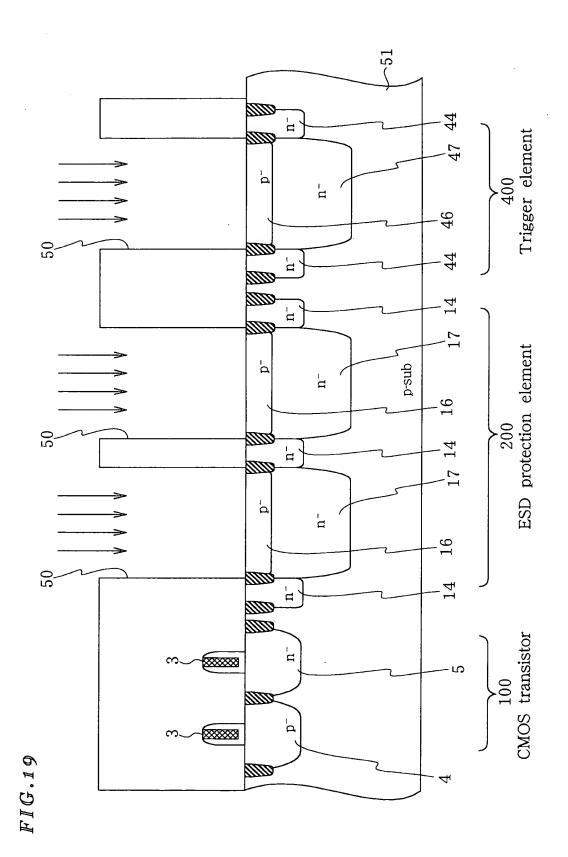


FIG.17







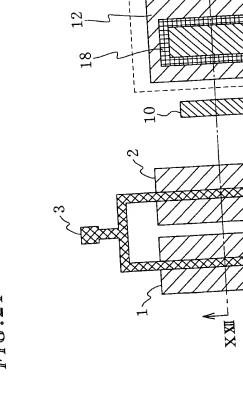
 \sim 51 44 40 400 Trigger element \mathbf{n}^{-} 46 44 40 n. 17 200 ESD protection element qns-d \mathbf{n}^{-} n_ n_ 16 100 CMOS transistor **∞**

FIG.20

Trigger element

230 ESD protection element

> 100 CMOS transistor



and the semilar data in the management of

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FIG.21

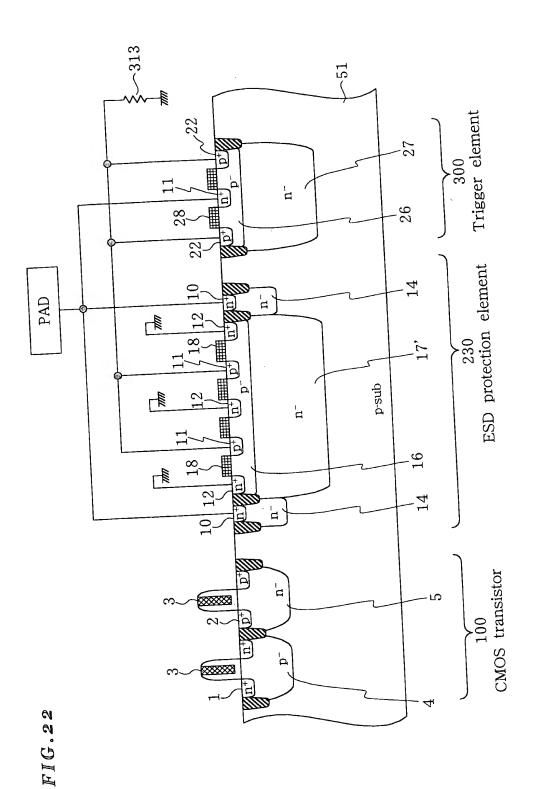
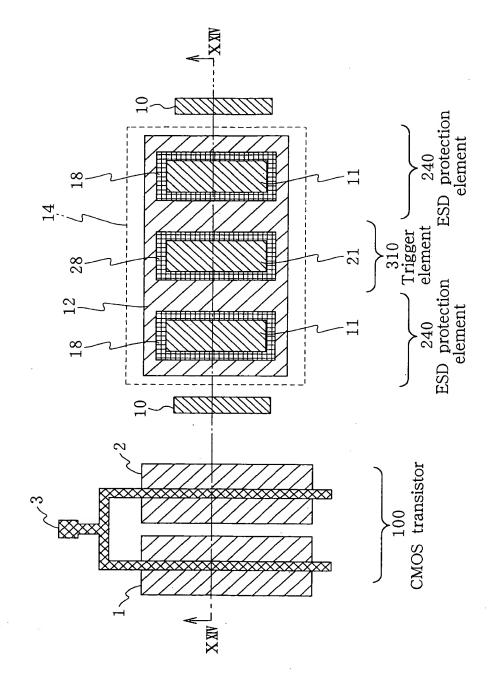
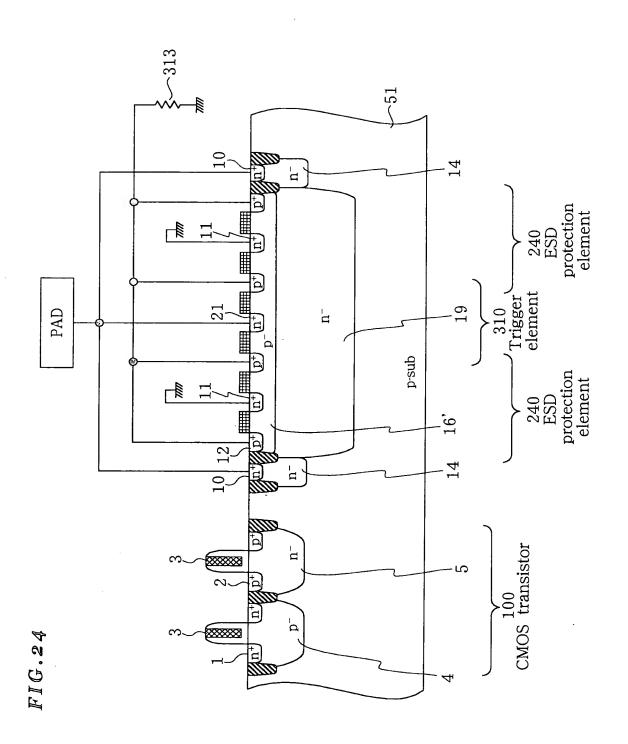


FIG.23





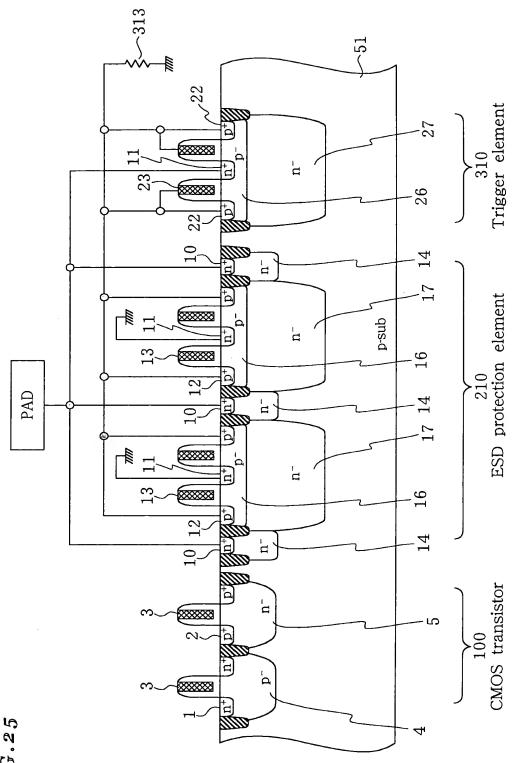
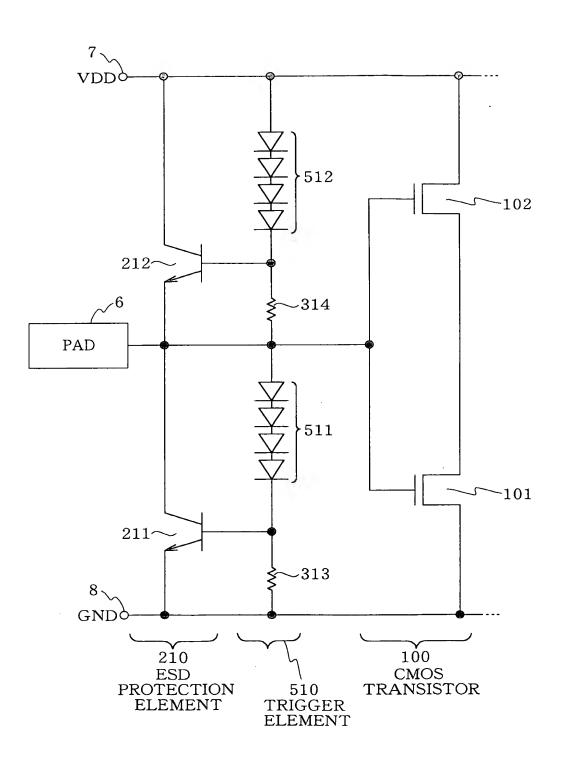
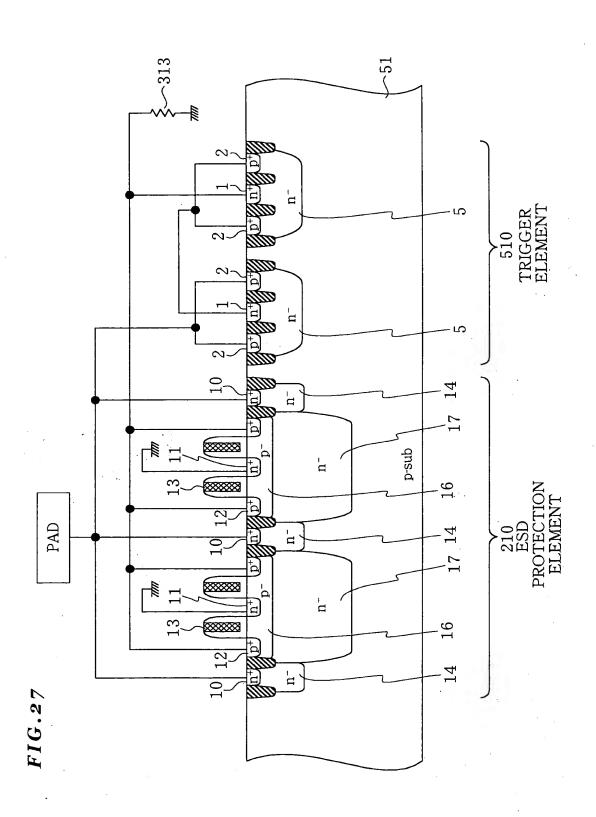
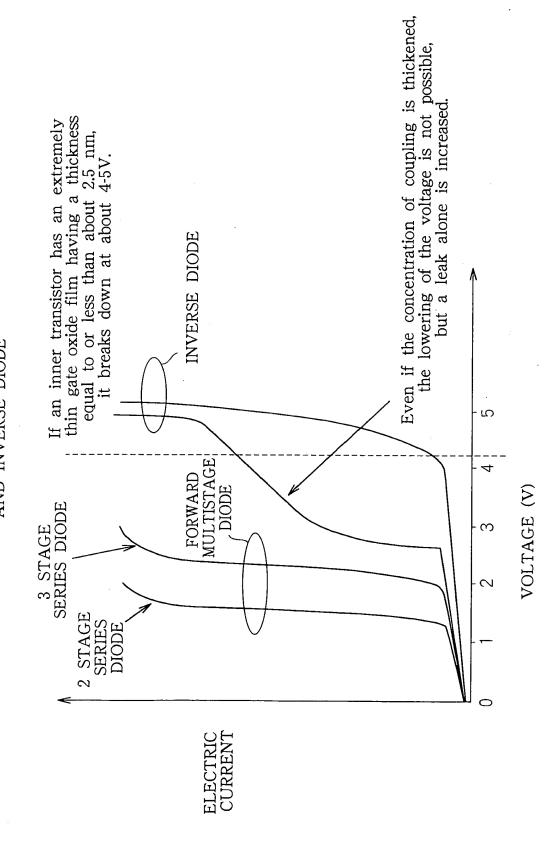


FIG.26





COMPARISON OF FORWARD SERIES CONNECTION DIODE AND INVERSE DIODE



GATE INSULATION FILM BREAKDOWN VOLTAGE OF INNER CMOS TRANSISTOR

LONGITUDINAL BIPOLAR TRANSISTOR OPERATING VOLTAGE

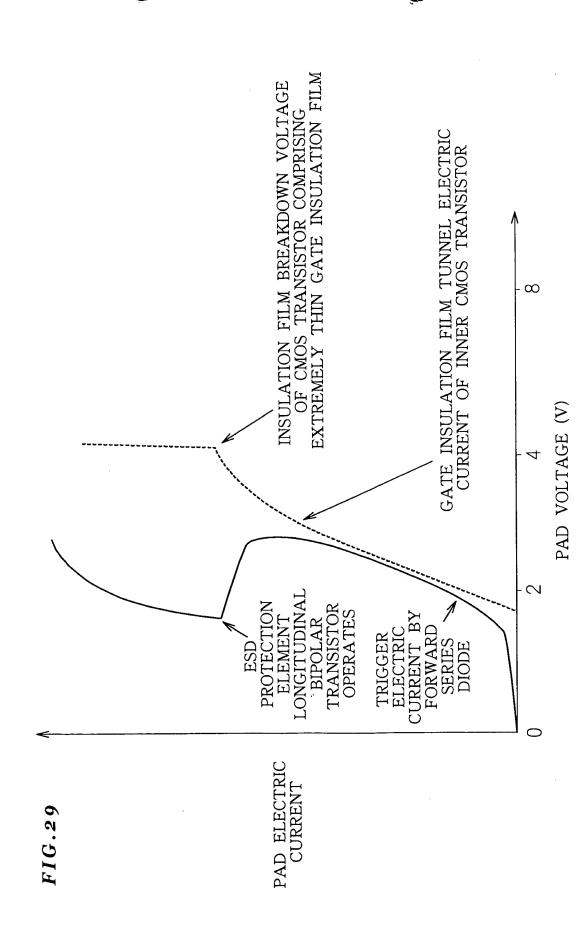
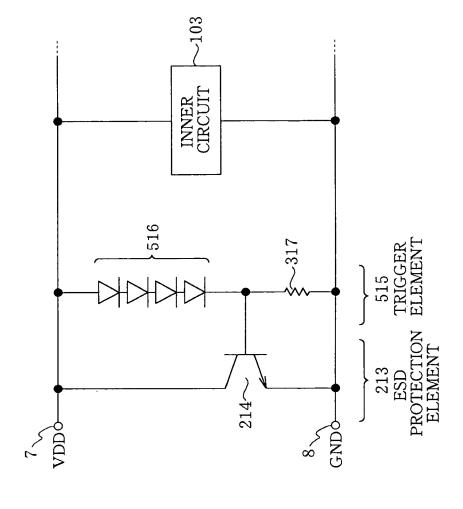


FIG.30



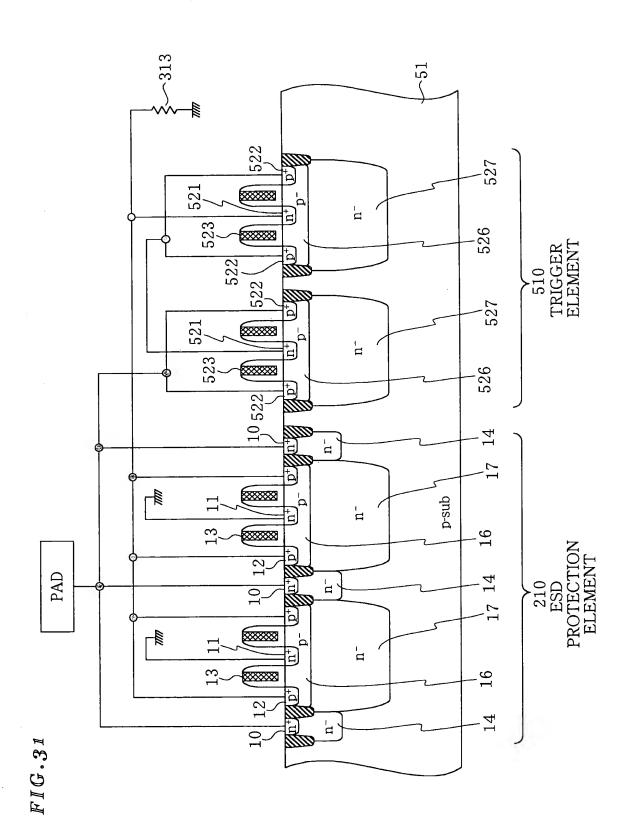
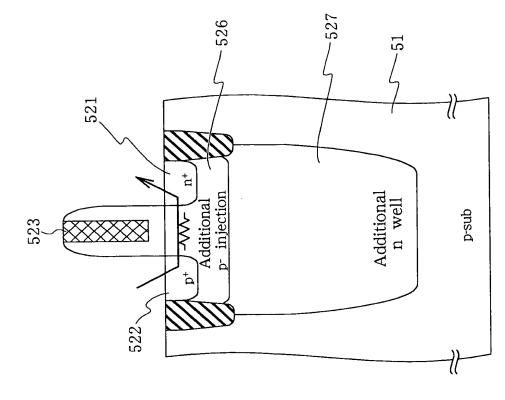


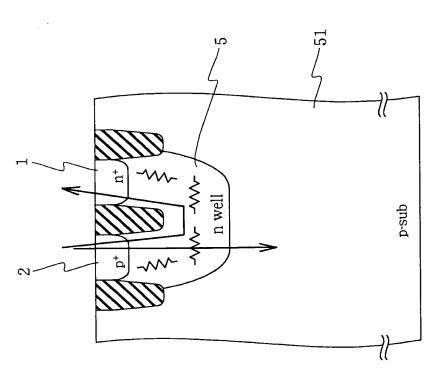
FIG.32(a)

DIODE COMPRISING p+LAYER/ n well FABRICATED BY EXISTING CMOS PROCESS

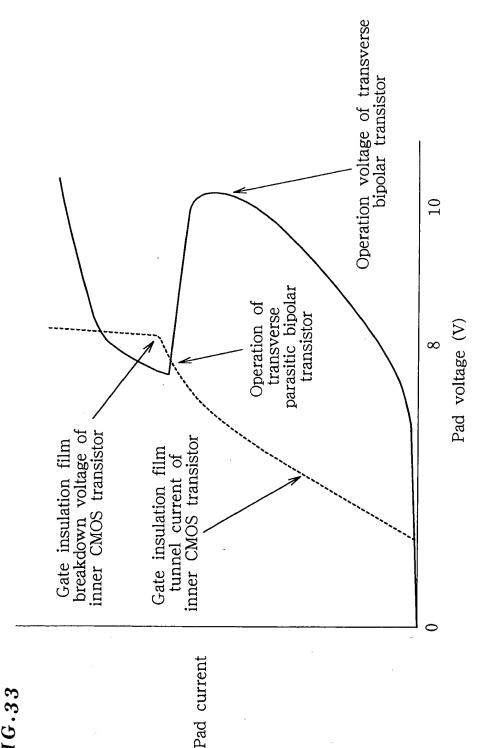
FIG.32(b)

DIODE UTILIZING ONE PORTION OF LONGITUDINAL BIPOLAR TRANSISTOR









Operation voltage of transverse < gate insulation film breakdown bipolar transistor < voltage of inner CMOS transistor